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AN ADVANCED PWM TECHNIQUE FOR LOW LOSS PURE SINE DC/AC CONVERTER

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Abstract- *PV arrays are used to capture the solar energy and generate a direct current which is then converted to an alternating current compatible with the grid. The ever-increasing reliance on electronic appliance which utilizes AC power focus the problems associated with the unexpected loss of power from DC/AC conversion. The system performing the DC to AC conversion must exhibit the highest efficiency to reduce unnecessary waste. A unique solution is to apply Unipolar PWM modulation to the DC/AC inverters to reduce the power loss. In the present study, the Unipolar Pulse width modulated (PWM) adaptive intelligent Power converter (inverter) has been designed and developed, where the input DC power from PV array has been digitized to produce loss less Pure sine wave to the load.*

keywords: Unipolar SPWM, DC/AC Converters, Full Bridge Topology, Microcontroller, and Photovoltaic System.

1. INTRODUCTION

Renewable sources of energy acquire growing importance due to massive consumption and exhaustion of fossil fuel. Among several renewable energy sources, photovoltaic arrays are used in many electrical appliances such as water pumping, industrial automations, home appliances, and grid connected PV systems. Solar inverter is a device that converts DC power source accumulated from PV arrays into AC power like utility grid. The inverter performing the DC to AC conversion must exhibit the highest efficiency not to waste the energy provided by the source. A unique solution is to adopt high-low unipolar PWM technique with A Full Bridge inverter topology to generate PWM sine wave pulses as shown in Fig.1 [1]. The semiconductor Power switches may be controlled to produce a multilevel unipolar PWM modulation.

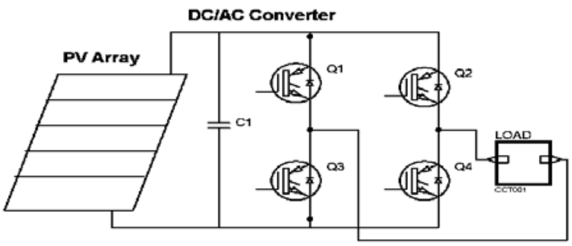

Fig.1: Solar inverter configuration using high-low unipolar PWM

2. Mode of Operation of the Unipolar Full Bridge

The very important criteria for a solar inverter are size, performance, reliability and cost, where the proposed unipolar switching DC/AC topology allows meeting the highest possible efficiency of the system, not only fundamental not to waste a precious energy but it is also essential for reducing the cost of producing electricity. There are two types of unipolar switching. Type one operates both switches pairs Q1, Q3 and Q2, Q4 at complementary high frequency (fig: 2). Type two uses a high frequency for one pair Q1, Q2 and line frequency for the other pair Q3, Q4 of switches. The proposed method is a type two unipolar PWM inverter .

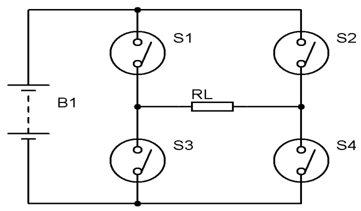

Fig. 2: Full Bridge Inverter Topology

The switching pattern is shown in tables I and II below where Vsine and Vtri are the sine wave and triangular wave control signals respectively [1].

Table 1: Complimentary Unipolar Switching - TYPE 1

Switch	State	Signal
S1	On	Vsine>Vtri
S2	On	–Vsine<Vtri
S3	On	–Vsine>Vtri
S4	On	Vsine<Vtri

Vo varies from Vdc to 0 or –Vdc to 0 and all four switches follow high frequency signals.

Table 2: High-Low Unipolar Switching - TYPE 2

Switch	State	Signal
S1	On	Vsine>Vtri
S2	On	Vsine<Vtri
S3	On	Vsine>0
S4	On	Vsine<0

S1, S2 are high frequency and S3, S4 are low frequency at output frequency, such as 50 Hz.

During positive output half cycle, Q1 is sine pulse width modulated (sine PWM) while Q4 is kept on. During negative output half cycle, Q2 is sine pulse width modulated while Q3 is kept on. The switching frequency of the high side and low side IGBTs are 20 kHz and 50 Hz, respectively.

3. Description of the Proposed Design

Proposed technique is unique of its type because it is implemented through a low cost RISC microcontroller PIC16F685. The operating speed supported by its 8 MHz internal clock. The reference voltage of the ADC module is 5 V with the resolution of 10 bits. High frequency (20 kHz) SPWM can be generated using its Enhanced PWM module. A filter is designed at the output stage of the inverter to translate PWM into a sinusoid wave. Voltage regulation is one of the important features of the inverter that implemented with PID feedback loop [2].

The sinusoidal Pulse Width Modulation (SPWM) was generated by creating a reference sine lookup table inside the memory of 8bit RISC microcontroller using the equation (Eq1) for half cycle.

$$vref = Vpik\,(\sin *\ 2\pi K)/N$$

with k = 0.... N/2 - 1 and N = the number of samples per cycle. For the Vp = 255 and N = 64 samples per cycle, this yields the following table entries. Only 32 entries are generated as the negative-going half cycle will be generated from the negative of the first 32.

Vref = 0, 25, 50, 74, 98, 120, 142, 162, 180, 197,212, 225, 235, 244, 250, 254, 255, 254, 250, 244,235, 225, 212, 197, 180, 162, 142, 120, 98, 74, 50, 25. A timer interrupt is generated for 64 times per cycle, then on every trigger of interrupt it calls Vref points one by one serially to the PWM register PR2 of microcontroller, hence Sine Modulated PWM generated respect to the reference lookup table [3]. First half cycle of SPWM is applied to Q1 (Fig.2) and its corresponding switch Q4 is turned on ; after 10ms Q2 is fed second half cycle of SPWM and Q3 is turned on. To keep output voltage constant, an infinite loop checks the output voltage through 10bit ADC, then the error signal send to the PID algorithm. The output of PID algorithm defines the duty of SPWM. The flow chart is given below.

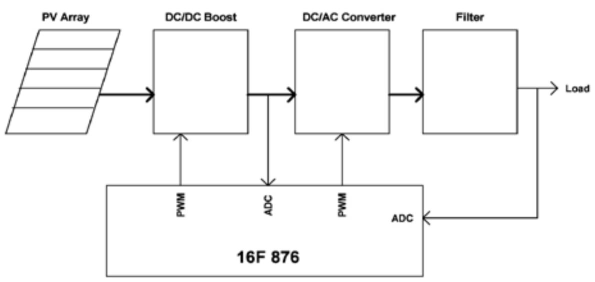

Fig. 3: Block diagram of inverter under investigation

4. Flow Chart

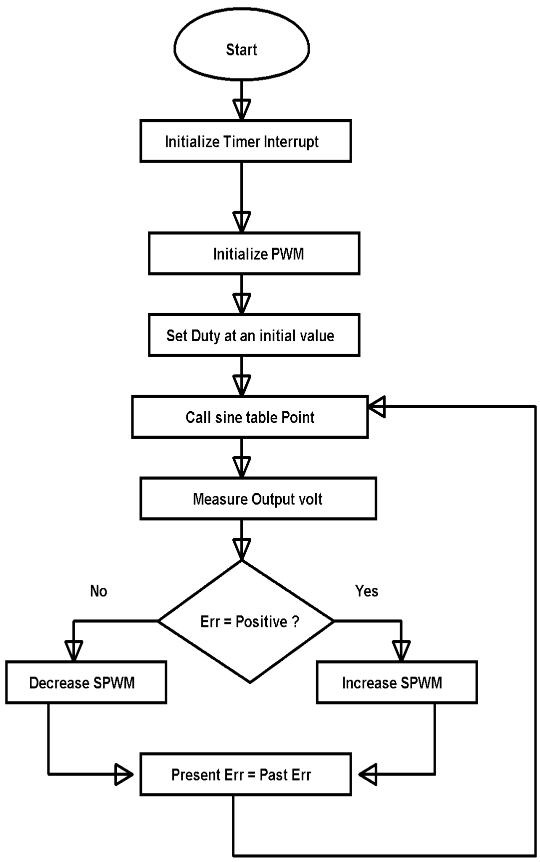

Fig.3: Flowchart of the proposed PWM algorithm

5. System Modeling

The block diagram of the inverter system under investigation is shown in Fig.6.The Block of solar inverter system is Designed and Simulated in Proteus ISIS. Our designed system parameters are given in Table1

Table 3: System Parameters

Power rating	400VA
Output voltage (regulated)	220V
Output current (Pick)	1.8
Inv switching frequency	20Khz
Output frequency	50Hz
Max load (tested)	160 Ohms

6. System Performance

A prototype Inverter system has been developed using the above-described method and tested in the laboratory. The inverter was tasted with a 200 W maximum power and both linear and nonlinear load. Various combinations of technologies are compared in terms of efficiency as a function of output power. The study is also performed with different operating frequencies to better measure the impact of the switching losses of the different fast switches.

The system efficiency is defined as:

$$\eta = \frac{Po}{Pin} = \frac{Po}{Po + Pd}$$

Where and are the DC/AC converter input and output Power, respectively, while is the power loss. The power loss consists of the IGBT and diode conduction and switching losses, the inductor core and copper losses and the control system power consumption. The theoretical values were calculated using data given by the manufacturers of the circuit elements. The theoretical and measured efficiency for various output power levels is shown in Fig.7. It is seen that the efficiency is quite high and relatively constant for a wide output power range.

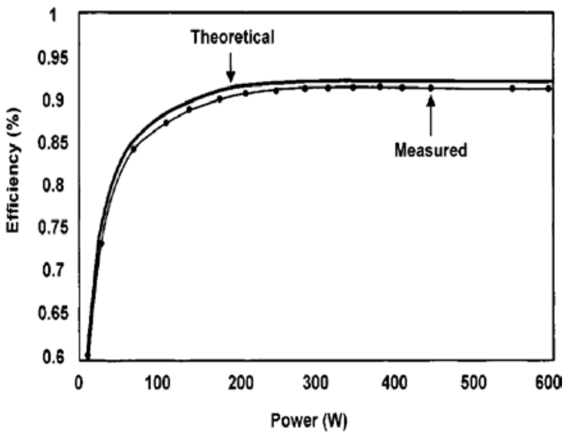

Fig.5: System efficiency various load.

The topology introduced, is simpler and easily implement able with PIC16F685. A 50Hz sinusoid with unity magnitude is multiplied with the impulse train of 20000Hz so that one complete cycle of sinusoid contains 400 impulses as shown in Fig.2.

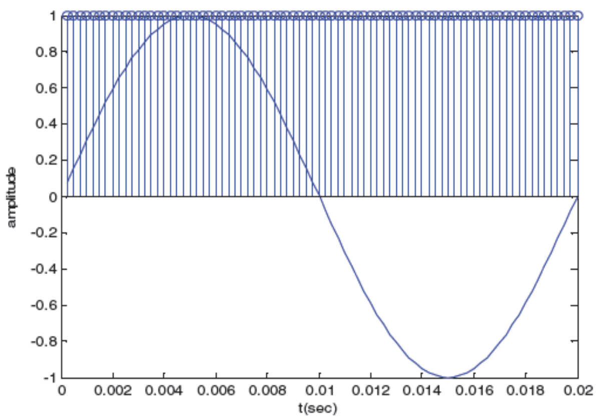

Fig.6: Unit impulse train and normalized sine wave

Output signals form controller to IGBT H Bridge is simulated in Proteus ISIS FIG.7. Q1 and Q2 are fed the switching frequency of 20 Khz where Q3 and Q4 is given line frequency [4].

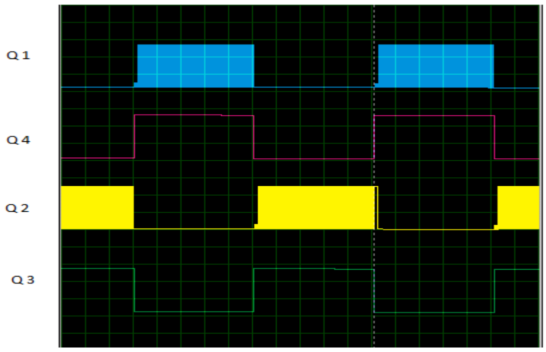

Fig.7: Simulation of switching pattern

Simulated output of high low unipolar PWM from H Bridge is shown Fig.8

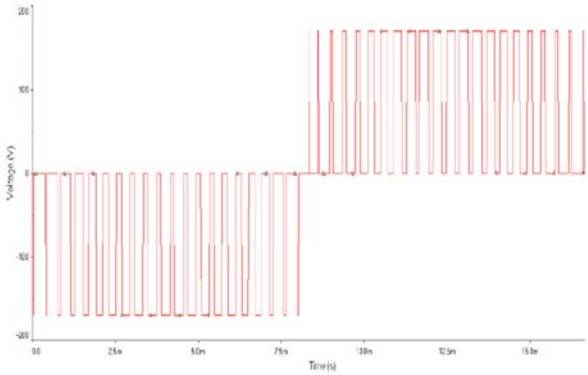

Fig.8: High low Unipolar PWM H-Bridge output without filter

Real output of inverter with mix mood load (both inductive and resistive) is given shown in Fig.9.

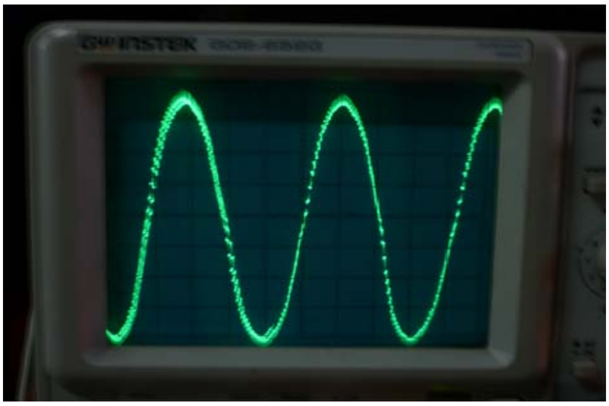

Fig.9: Real output of inverter with mix mood load

Each leg of the H-Bridge is driven using a high voltage gate driver IC, IRS2106SPBF, with bootstrap power supply technique for the high side. Using IRS2106SPBF eliminates the requirement for an isolated power supply for the high side drive. This translates into increase efficiency and parts count reduction of the overall system [5].

7. Advantages of the Proposed H-Bridge Topology and Switching Technique

High efficiency since Q1 and Q2 co-pack diodes are not subjected to the freewheeling current and Q3 and Q4 have majority of conduction loss and very little switching loss. No cross conduction possibility since switching is done on diagonal device pair only at any time (Q1 and Q4 or Q2 and Q3). Operate from single DC bus supply eliminating the need for a negative DC bus [6]. IGBTs are driven using high voltage gate driver IC with bootstrap technique. Bootstrap capacitors are used so there is no separate floating power supply required for the high side drive.

8. Conclusion

Unipolar switching full bridge topology offers the best efficiency performance in modern solar converters with the low conduction and fast switching devices. Each of the device brings its own advantages to the system, either low conduction or fast switching properties while its drawbacks have no or minor impact to the system [7]. MOSFETs or IGBTs will allow to reach efficiencies better than 99% and to perform the maximum that is technically feasible.

9. References

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